General Description:

LPD6803 is a 3 channel constant-current driver and grey-level modulate output , it uses advanced high-voltage CMOS technology, provide 3-way, designed to meet the needs of driving function in the LED lighting system, especially in the dissociation with mutual grey level in the full-colour lighting system..

LPD6803 includes serial shift register and concatenation driver circuit, grey level data shift into serial shift register in the clock, and transfer saving , it transfer to interface 3 after pulse-width modulate ,then output, serial shift register and grey-level counter can be controlled by different clock signal. In the meantime, LPD6803 driver data signal and control signal , and output next circuit.

Features:

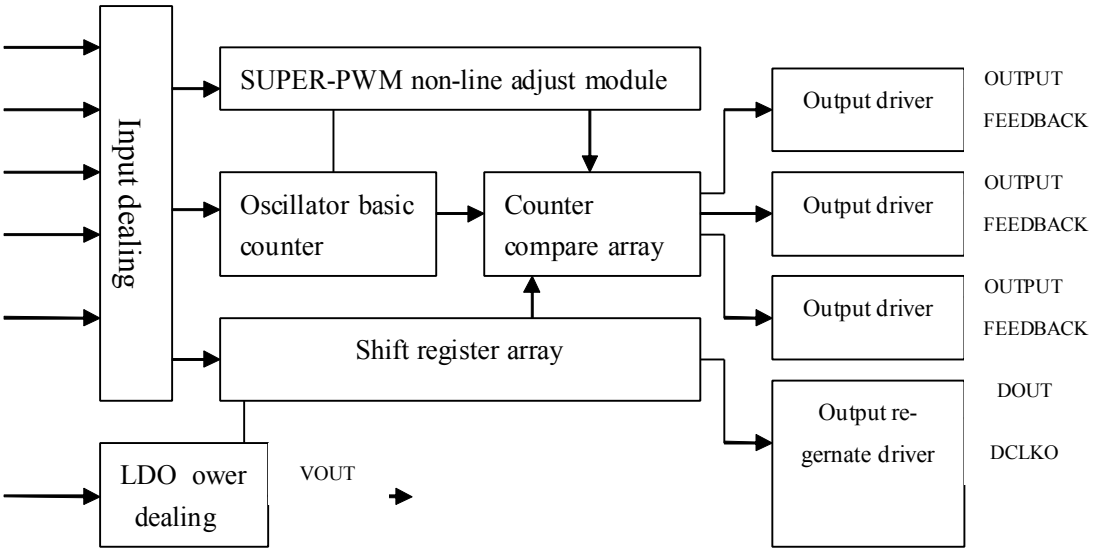
- ◇ 3channel driver output, maxim current per channel is 45mA, LED light voltage can reach 12V.
- ◇ Output adopt In-Rush online feedback contant-current driver structure, compatible with constant-voltage module, it also can contact outside equipment and transfer to higher voltage or current output driver.
- ◇ Built-In LDO voltage-stabilizing circuit, voltage range is 3-8v, and have 5V stabilizing voltage output.
- ◇ Adopt self-add token-ring technology dual shift line, shift clock can reah 24MHz.
- ◇ Directly input grey-level data, it is transfer to 256 output with reverse-gamma regulator after inside SUPER-PWM technology, e.g, adopt built-in oscialator as grey-level clock, it support FREE-RUN module output, especially can be used in low-cost controller.
- ◇ Data clock signal is drived strongly to next chip to enhance level after built-in phase-lock circuit.
- ◇ High-voltage CMOS technology, industrial design, with extra-good interference immunity
- ◇ With SOP16/QFN16 Pb-Free package, meet the requirement of Rohs , also can provide COB package or DIE.
- ◇

Footprint:

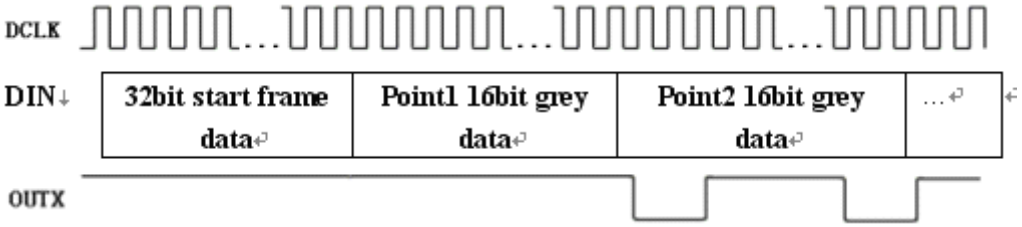
LPD6803 footprint function description:

Foot	Name	Function
1	DIN	Serial data input, built-in voltage pull-up
2	GMODE	Grey-level regulate mode: GMODE=1,adapt line modulate,GMODE=0,adapt re-Gama 256 grade non-line regulate,built-in voltage pull-up
3	OMODE	Control output polarity: OMODE=1, output is in-constant current/voltage drive mode,CMODE=0, output is out drive mode,voltage built-in pull-up
13	CMODE	choose inside grey clock GCLK, CMODE=0, GCLK=DCLK, CMODE=1, GCLK= inside oscillator output, built-in pull-up
4	DCLK	Serial data clock input, built-in pull-up
5,7,11	OUT1,OUT2,OUT3	3-way driver output
6,8,10	FB1,FB2,FB3	Feedback input in constant current state
15	DOUT	Serial data output, after inside strongly drive
12	DCLKO	Serial clock output, after inside pll and strongly drive
16	VCC	LDO power, range is 4.5v---8v
14	VOUT	when VCC>5V, 5V stable voltage output, when VCC<5V, VOUT=VCC, can be used as inside working voltage, suggest outside contact a 0.01uF----0.1uF capacity
9	GND	Ground

Function Block:



Basic timing sequence



A. First shift in 32bit "0" as start frame, then shift in all data frame, start frame and data frame both are shift by high-bit, every data is input on DCLK rising edge.
B. The first data frame is corresponding LED light nearest from shift-in polar, its format includes 1bit as start "1" plus 3 groups 5bits grey level.
C. Turn shift in all data, add append pulse of corresponding point, new data start valid.

Function features:

- Limited parameter:

Parameter	Symbol	Range	Unit
Supply voltage	VDD	3-8	V
LED light voltage	VLED	3-12	V
Data Clock Frequency	FCLK	25(compatible with grey level at 10)	MHZ
Maxim Driver Current	IOMAX	45 at constant voltage, 30 at constant current	mA
channel current error	DIO	chip inside <5%, between Chip <6%	%
power consumption	PDMAX	600	mW

Soldering Temp	TM	300(8S)	℃
Working Temp	TOP	-40 ---+80	℃
Saving Temp	TST	-65 ---+120	℃

● Suggested working parameter:

Parameter	Symbols	Range	Unit
Supply Voltage	VDD	5-7.5	V
voltage-stabilizing output voltage	VOUT	5±5% (customer data)	V
Input Voltage	VIN	-0.4～Vout+0.4	V
Data clock frequency	FCLK	0-15	MHZ
Clock high-level voltage width	TCLKH	>30	ns
Clock low-level voltage width	TCLKL	>30	ns
Data build time	TSETUP	>10	ns
Data keep time	THOLD	>5	ns
Power comsumption	PD	<350	mW
Working Temp	TOP	-30～+60	℃

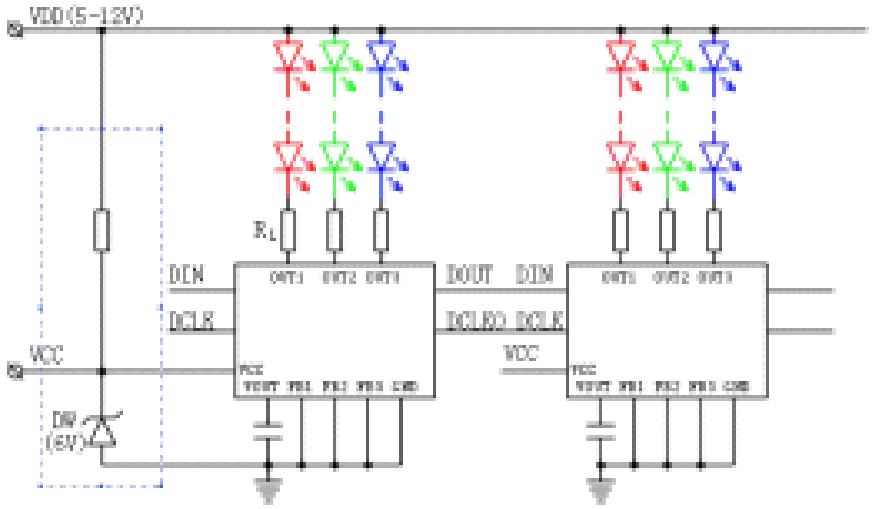
●Timing sequence parameter

Timing sequence parameter:(T=25℃,VDD=5V, OMODE=1,GMODE=0,CMODE=1)

Parameter	Symbols	Testing condition	Range	Unit
Maxim up and down time of innput signal	TR	VDD=5V	<500	ns
	TF		<400	
Up and down time of concatenation output signal	TTLH	CL=30pF,RL=1K	<15	ns
	TTHL		<15	
Maxim delay time of concatenation output	TPD	CL=30pF,RL=1K	<12	ns
	TCO		<12	
Min PWM width of driver output	TONMIN	IOUT=20mA	200	ns
Maxim open and close time of driver output signal	TON	IOUT=20mA	<80	ns
	TOFF		<80	

Typical application circuit:

>Inside constant voltage driver (compatible with ZQL9712) mode:



This mode (OMODE=high voltage level or dangle)is suitable used in the situation which VDD not higher 12V and current on each way not huge 400mA, if VDD<7.5V, you can ignore those parts in blue dashed above chart, directly contact VDD to VCC.

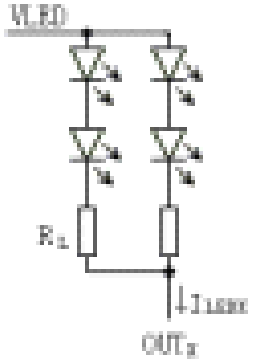
Current regulator resistance count: RL=(VDD-VLED-VOUT)/ILED

Here: RL is limit current resistance value, VDD is LED light supply voltage, VLED is LED light voltage when it breakover, VOUT is saturation voltage of the output polar to the grand(about 0.4v –0.8v), ILED is LED working current(normally no bigger 20mA)

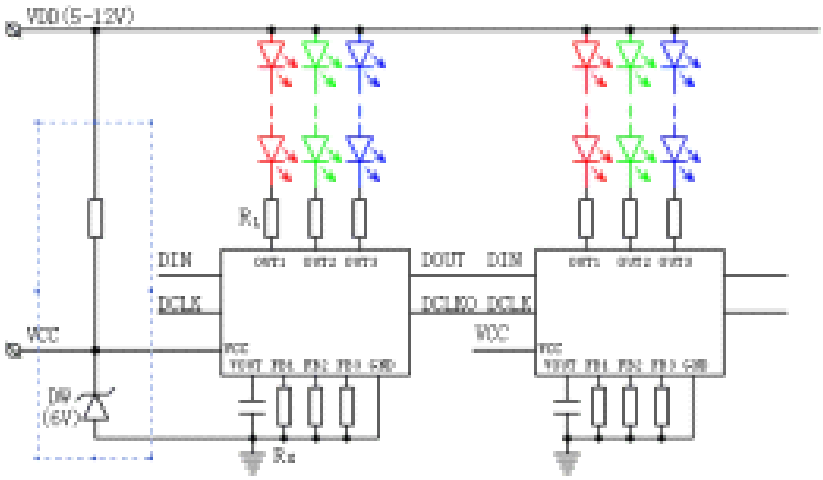
LPD6803 has strong driver capability , in the many LED apply situation, we can adopt the contact of "First serial then parallel" (see right chart), but we must pay attention on power consumption can not exceed maxim value PDMAX:

PD=ILED1*VOUT1+ILED2*VOUT@+ILED3*VOUT3+PIC

Here : PIC is IC basic power consumption , normally not exceed 25mW.



>Inside constant current driver mode:



This mode (OMODE=high level or dangle) application is same as above , only add a RX at FBX polar which regulate current, this LED current is decided by RX: ILED≈0.7V/RX

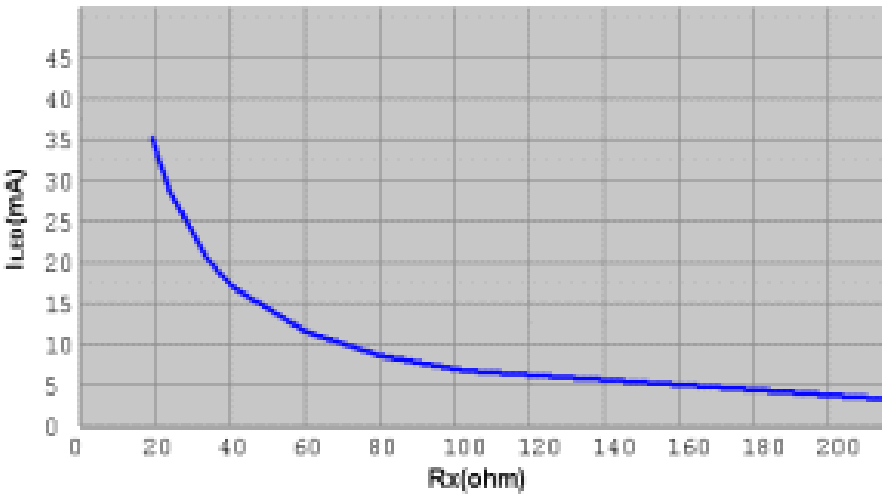


Chart1: Iled –Rx curve

Pls note that only can keep constant current when voltage to the grand VOUT is at the range of 1.1---6v. that is meet:

VLED+6V+ILED*RL≧VDD≧VLED+1.1V+ILED*RL

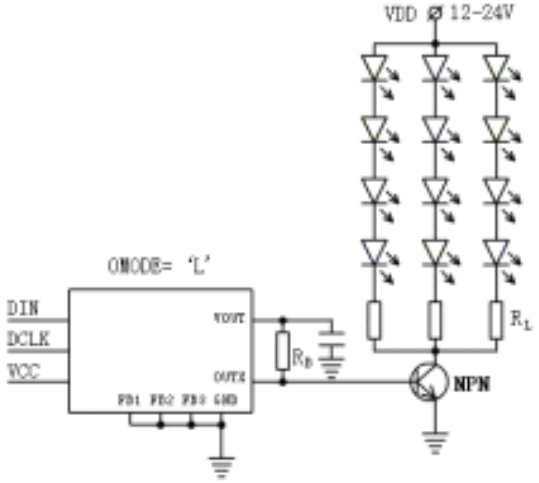
Circuit value must notice that power consumption PD won't exceed its maxim value PDMAX.

PD=ILED1*(Vout1-0.7V)+ILED2*(Vout2-0.7V)+ILED3*(Vout3-0.7V)+PIC

Here ILED1/ILED2/ILED3 is respectively current which passed each LED light, and Vout1/Vout2/Vout3 is respectively each output voltage to the grand .

Rl is normally tens Ohm, no any effect to ILED, it is ok if no Rl, but a suitable
RL can be help to share chip power consumption PD, can improve working stability.

- **outside constant voltage drive mode:**



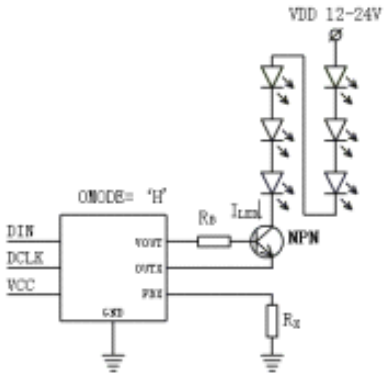
This mode (OMODE=grand)is suitable in many LEDs situation or high light voltage, Actually, serials LEDs are drived by OUTx which control NPN transistor whish is outside contact to .

Limited current resistance count: Rl=(VDD-VLED-VCE)/20mA

Here transistor works in switch area, Vce is saturate voltage of transistor, normally is 0.5v---0.8v, base resistance Rb can be set at 2k—5k, other signal contact mode are same as prior mode.

This mode often is used in multiple way "first serial then parallel" connection, because all LEDs won't light on this once any LED switch off in serial route,
So we must obey this connection rule: LED qty can not be too many in serial route (normally 3-6pcs), and can not be too less in parallel route. This can reduce
Accidents influence of one broken LED, and will make limited resistance to zero, Make one huge power resistance to many small power ones, make central installation to disperse one, it is good to conduct heat and make lights more compaction.

Outside constant current drive mode:



This mode (OMODE=high level voltage or dangle) is suitable in several LEDs and VDD is higher than 12V, its essence is to higher capability of withstand voltage in the
time of keeping characteristic of constant current in the circuit.

Current passed LED : ILED= Io*β/(β+1)

Here Io is current value related to chart 1, transistor is working in amplify area,
Bis amplify multiple, whenβ is bigger, above formula can be near equal to :
Iled = Io (bias resistance RB can be get as 5k)

Highest capability of withstand voltage VDD is decided by VCEO on NPN transistor, normally is 25V or above.

Linking signal driver and link:

Considering of that the distance between of chips may be long long, DOUT and DCLKO
Output terminal is designed to push-pull strong drive circuit, after testing, it can drive 6meters length signal line when clock is 2M, to prevent signal echo, normally, pls serial a 50Ω resistance at DOUT and DCLKO, then output to next step.
Control circuit and software reference design:

Via set CMODE, LPD6803 grey level counter can adapt DCLK as clock(CMODE=0),
Also can adapt built-in 1.2M(error ±15%)osscilator output of as clock(CMODE=1 Or dangle), prior one is normally used in those based on CPLD/FPGA high cost control system, later one is often used in low cost MCU control system.

In CMODE=1 mode, MCU write display data into chip via SPI or two GPIO interface line,
then each chip will automatically produce drive output with related duty cycle according to input grey level value, after data transfered, MCU can deal with

other
task, during this time, each LPD6803 will continue keeping original duty cycle drive output(FREE-RUN mode), till MCU send out next updated data.

Notice: after all data are input in chip on the up-edge of DCLK, it may need send more DCLK pulse (DIN=0), on principle, how many group point in the transfer link, how many related pulse need to be sent out, it is important to which later chip built-in PLL re-gernate circuit can work in gear.

To make LPD6803 produce more particularity grey level by less data, when GMODE=0/
CMODE=0, built-in SUPER-PWM can change 5 bit data into non-line 256 grade grey output, minimum open width is 1T, maxim open width is 256T (T is grey clock cycle)

When GMODE=1 or dangle , output is line 32 grade grey, minimum open width is 4T, and maxim open width is 128T.

C51 example:

```
//SDO, SCLK is data and shift output, bit variability ,nDots is light qty
// this program is only suitable in GMODE=1,CMODE=1 situation.
// first output 32 “0” start frame
   SCLK=0;
    SDO=0,
    For (i=0;i<32;i++){SCLK=1;SCLK=0;}
// then output nDots data, here suppose each point colour are(dr,dg,db)
//dr,db,dg is red, green and blue grey level 0-31
  For (i=o;i<nDots;i++)
  { SDO=1;SCLK=1;SCLK=0;              //first output one “1” as start bit
     //output 5 bits red data
     Mask=0x10;
     For (j=0;j<5;j++)
     { if (mask &dr) SDO=1;
       Else          SDO=0;
       SCLK=1; SCLK=0;
       Mask>>=1;   }
// output 5 bits green data
  Mask=0x10;
  For (j=0;j<5;j++)
  { if(mask &dg)SDO=1;
    Else        SDO=0;
    SCLK=1;SCLK=0;
    Mask>>=1;  }
```

```
//output 5bits blue data
Mask=0x10;
For (j=0;j<5;j++)
{ if(mask & db) SDO=1;
  Else          SDO=0;
  SCLK=1;SCLK=0;
  Mask>>=1;   }
}
// after output all nDots data, need add nDots pulse
SDO=0;
For (i=0;i<nDots;i++){SCLK=1;SCLK=0;}
//transport data finish
Delay();
//here add some delay , or transfer to other dealings, after some time(say 1/30 second), then fresh again.
```

LPD6803 duty cycle table:

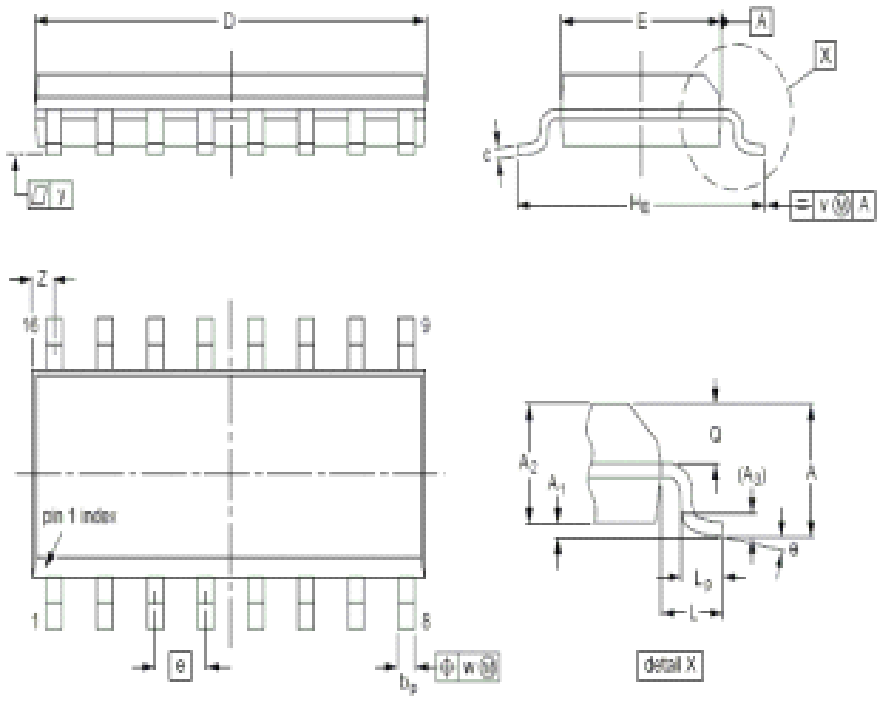
input data	output duty cycle (unit: 1/256)
0	0
1	1
2	3
3	5
4	8
5	12
6	16
7	21
8	26
9	32
10	38
11	45
12	52
13	60
14	68
15	76
16	85
17	95
18	105
19	115
20	125
21	136
22	148

23	160
24	172
25	185
26	198
27	211
28	225
29	239
30	254
31	256

Memo: this table is output duty cycle related to 32 grade grey level when GMODE=0,

Its data is revised curve related to GAMMA=1.8

SOP16 package dimension:



DIMENSIONS (inch dimensions are derived from the original mm dimensions)

UNIT	A max.	A_1	A_2	A_3	b_p	c	D(1)	E(1)	e	H_E	L	L_p	Q	v	w	y	Z(1)	θ
mm	1.75	0.25 0.10	1.45 1.25	0.25	0.49 0.36	0.25 0.19	10.0 9.8	4.0 3.8	1.27	6.2 5.8	1.05	1.0 0.4	0.7 0.6	0.25	0.25	0.1	0.7 0.3	8° 0°
inches	0.069	0.010 0.004	0.057 0.049	0.01	0.019 0.014	0.0100 0.0075	0.39 0.38	0.16 0.15	0.050	0.244 0.228	0.041	0.039 0.016	0.028 0.020	0.01	0.01	0.004	0.028 0.012	

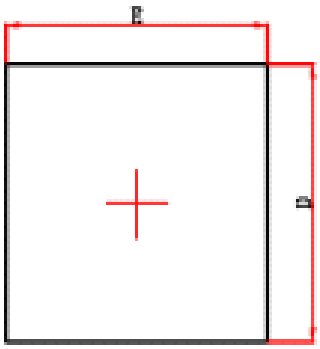
Note

1. Plastic or metal protrusions of 0.15 mm maximum per side are not included.

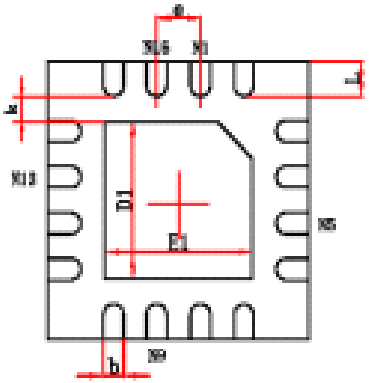
OUTLINE VERSION	REFERENCES				EUROPEAN PROJECTION	ISSUE DATE
	IEC	JEDEC	EIAJ			
SOT109-1	076E07S	MS-012AC				~~96-01-23~~ 97-05-22

QFN16 package dimension:

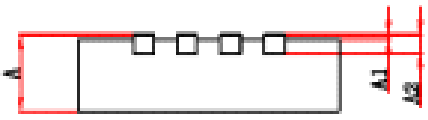
QFNWB3×3-16L(P0.50T0.75/0.85) PACKAGE OUTLINE DIMENSIONS



Top View



Bottom View



Side View

Symbol	Dimensions In Millimeters		Dimensions In Inches	
	Min.	Max.	Min.	Max.
A	0.700/0.800	0.800/0.900	0.028/0.031	0.031/0.035
A1	0.000	0.050	0.000	0.002
A2	0.153	0.253	0.006	0.010
D	2.900	3.100	0.114	0.122
E	2.900	3.100	0.114	0.122
D1	1.600	1.800	0.063	0.071
E1	1.600	1.800	0.063	0.071
k	0.200MIN.		0.008MIN.	
b	0.180	0.300	0.007	0.012
e	0.500TYP.		0.500TYP.	
L	0.300	0.500	0.012	0.020