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Achieving Higher ADC Resolution Using Oversampling

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INTRODUCTION

An Analog-to-Digital Converter (ADC) is an active interface between the analog and digital signal chains in an embedded system. An ADC converts analog signals into digital signals in electronic systems. The key feature of an ADC is the accuracy (resolution) it offers. The higher the desired accuracy, the higher the ADC cost.

Higher ADC accuracy is achieved by designing hardware to quantize the analog signal amplitude into the digital signal with a higher code-word length. Practical ADCs have finite word lengths.

To effectively strike a balance between system cost and accuracy, higher conversion accuracy is achieved by oversampling the low-resolution ADC integrated within a digital signal controller (DSC), and then processing the oversampled digital signal in software through a digital filter and a decimator. This processing scheme, which adds additional bits of accuracy to the 12-bit ADC conversion in a dsPIC® DSC, is explored in this application note.

THEORY OF OPERATION

As previously mentioned, ADCs transform analog signals into digital sample values. Analog signal amplitude is quantized into digital code words with a finite word length. This process of quantization introduces noise in the signal called “quantization noise”. The smaller the word length, the greater the noise introduced.

Quantization noise can be reduced by adding more bits into the ADC hardware design. This noise can also be reduced in software by oversampling the ADC and then processing the digital signal. The oversampling ADC method and a few associated terms are explained in the following sections.

ADC Voltage Resolution

Voltage resolution of an ADC is defined as the ratio of full scale voltage range to the number of digital levels that are accommodated in that range. It is a measure of the accuracy of the ADC. The higher the resolution, the higher the number of levels accommodated in the voltage range and, consequently, the lower the quantization noise, as shown in Equation 1.

EQUATION 1:

$$\textit{Voltage Resolution} = \textit{1 Least Significant bit (LSb) value} = \frac{\textit{full scale voltage range}}{2^N - 1}\left[\frac{volts}{level}\right]$$

where N is the number of bits or the word length

The smallest ADC step represents one Least Significant bit (LSb) value. For example, if the full scale measurement voltage range is 0 to 3 volts, and the ADC bit resolution is 12 bits, then the ADC voltage resolution can be calculated to be 0.7326 mV/bit.

This means the conversion of continuous voltages is noise free if the continuous voltage is an integral multiple of the voltage resolution. Any intermediate continuous voltage is rounded off to suit a voltage level that is an integral multiple of the voltage resolution, as shown in Figure 1. This introduces quantization noise, as shown in Figure 2.

FIGURE 1:

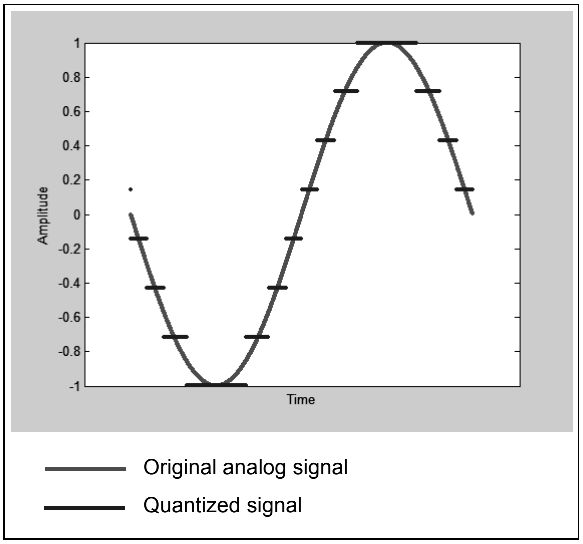
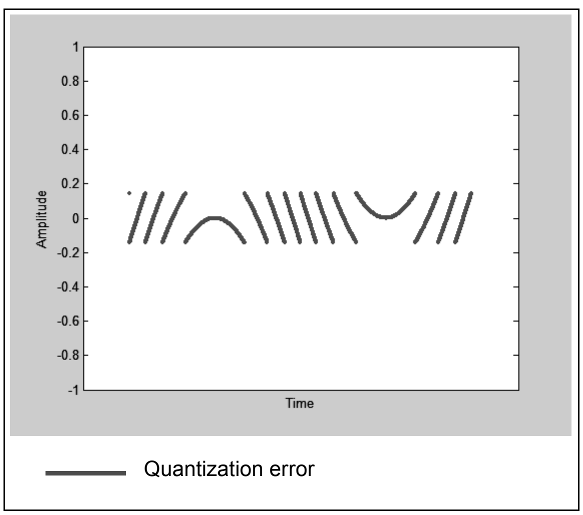


FIGURE 2:



The measure of the extent to which the signal is corrupted with quantization noise after analog-to-digital conversion is given by the signal-to-quantization noise ratio.

Signal-to-Quantization Noise Ratio

Signal-to-Quantization Noise Ratio (SNR_Q) is defined as the ratio of the root mean square value of the input analog signal to the root mean square value of the quantization noise. The SNR_Q of an ideal *N*-bit ADC is given by Equation 2.

EQUATION 2:

$$SNR_Q = 6.02N + 4.77 + 20\log 10(L_F)[dB]$$

where, N is the number of bits or the word length, and L_F is the loading factor, which is defined as the ratio of the root mean square value of the input analog voltage to the peak ADC input voltage.

When the input analog signal is sinusoidal $L_F = 0.707$, then SNR_Q is given by Equation 3.

EQUATION 3:

$$SNR_{Q-MAX} = 6.02N + 4.77 - 3 = 6.02N + 1.77[dB]$$

From Equation 3, it is clear that the improvement in the SNR of the ADC is 6.02 dB per bit. The higher the number of bits associated with the ADC, the higher the SNR_Q. For example, the $SNR_{Q\text{-}MAX}$ of a 12-bit ADC is 74.01 dB and that of a 16-bit ADC is 98.09 dB. Now we will explore how the SNR can be improved without increasing the word length of the ADC.

Oversampling ADC, Digital Filtering, Decimation and Dithering

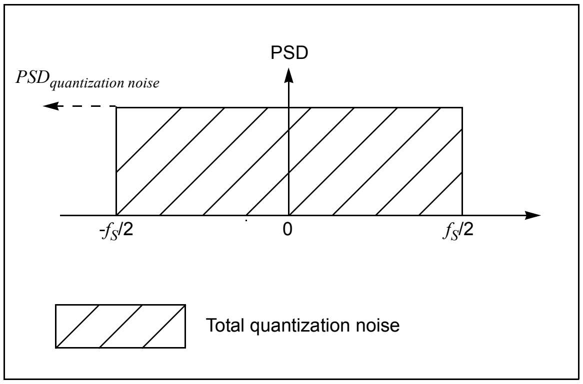
A cost-effective method of improving the resolution of the ADC is developing software to suitably process the converted analog-to-digital signal to achieve the same effect as a higher resolution ADC.

The Power Spectral Density (PSD) of the quantization noise with a flat spectrum, which gets added during an analog-to-digital conversion (see Figure 3), is given by Equation 4.

EQUATION 4:

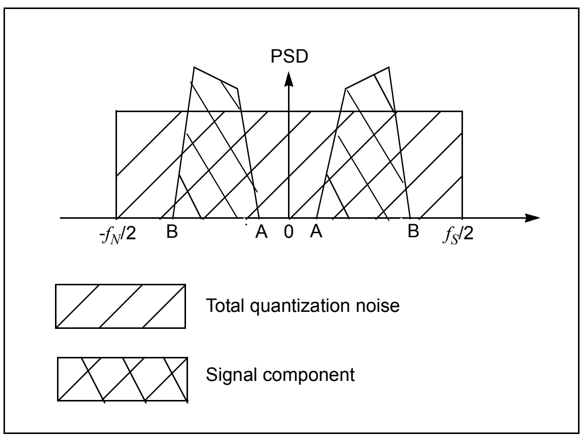
$$PSD_{quantization\ \mathrm{noise}} = \frac{(lsb\ value)^2}{12_{fs}}\left[\frac{W}{Hz}\right]$$

FIGURE 3: POWER SPECTRAL DENSITY OF QUANTIZATION NOISE IN AN IDEAL ADC



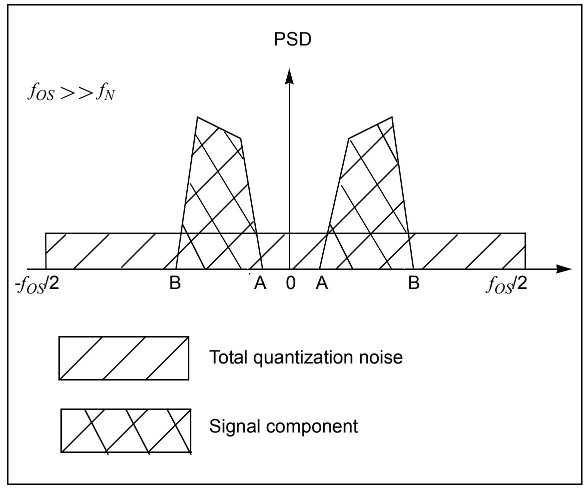
Power spectral density representation of the signal after an analog-to-digital conversion is seen in Figure 4.

FIGURE 4: POWER SPECTRAL DENSITY OF SIGNAL COMPONENT QUANTIZATION NOISE IN AN IDEAL ADC AFTER ANALOG-TO-DIGITAL CONVERSION



One way of reducing the *PSD* is by reducing the numerator (i.e., the LSb value), which can be achieved by adding more bit resolution to the ADC. Another method of reducing PSD is by increasing the denominator (i.e., by increasing the sampling frequency), which leads to oversampling. The power spectral density representation of the signal after analog-to-digital conversion and after oversampling is seen in Figure 5. The analog input signal is conveniently sampled at a sampling rate (f_{OS}) significantly higher than the Nyquist rate, f_N = 2B, with the help of the high sampling rate capacity of the ADC present in the dsPIC digital signal controller.

FIGURE 5: POWER SPECTRAL DENSITY OF SIGNAL COMPONENT QUANTIZATION NOISE IN AN IDEAL ADC AFTER ANALOG-TO-DIGITAL CONVERSION AND AFTER OVERSAMPLING



The SNR improvement after oversampling is given by Equation 5.

EQUATION 5:

$$SNR_{oversampling} = 10log\left(\frac{f_{OS}}{f_N}\right)[db]$$

The overall SNR is given by Equation 6.

EQUATION 6:

$$SNR_{overall} = 6.02N + 1.77 + 10log\left(\frac{f_{OS}}{f_N}\right)[db]$$

Suppose we have a *P*-bit ADC and *Q*-bit ADC, *Q* > *P*, the sampling factor is calculated as shown in Equation 7.

EQUATION 7:

$$\frac{f_{OS}}{f_N} = 10^{0.602(Q-P)}$$

Equation 8 shows how to achieve the SNR of a 16-bit ADC using a 12-bit ADC.

EQUATION 8:

$$SNR_{overall}\ \text{16-bit ADC} = SNR_{overall}\ \text{12-bit ADC with oversampling}$$

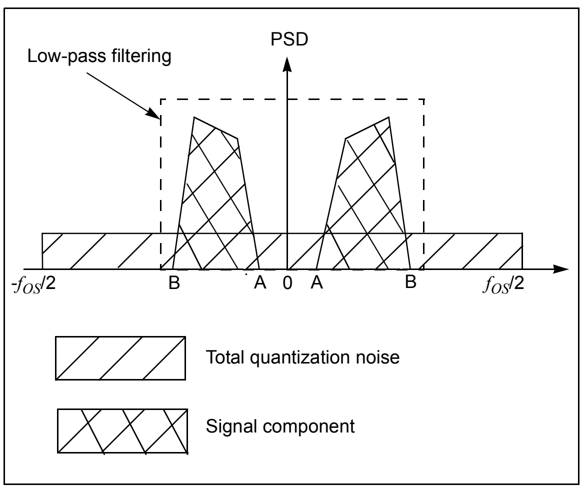
$$6.02 \cdot 16 + 1.77 = 6.02 \cdot 12 + 1.77 + 10log\left(\frac{f_{OS}}{f_N}\right)$$

$$\frac{f_{OS}}{f_N} = 255.8585 = 256$$

The analog signal should be oversampled at a rate of 256 times more than the Nyquist rate to achieve the SNR of a 16-bit ADC with a 12-bit ADC.

The oversampled analog-to-digital converted signal is low-pass filtered (see Figure 6) to alleviate the effects of quantization noise. The digital low-pass filter can be modeled as a FIR filter.

FIGURE 6: POWER SPECTRAL DENSITY OF SIGNAL COMPONENT QUANTIZATION NOISE IN AN IDEAL ADC AFTER ANALOG-TO-DIGITAL CONVERSION AND AFTER OVERSAMPLING WITH LOW-PASS FILTER RESPONSE



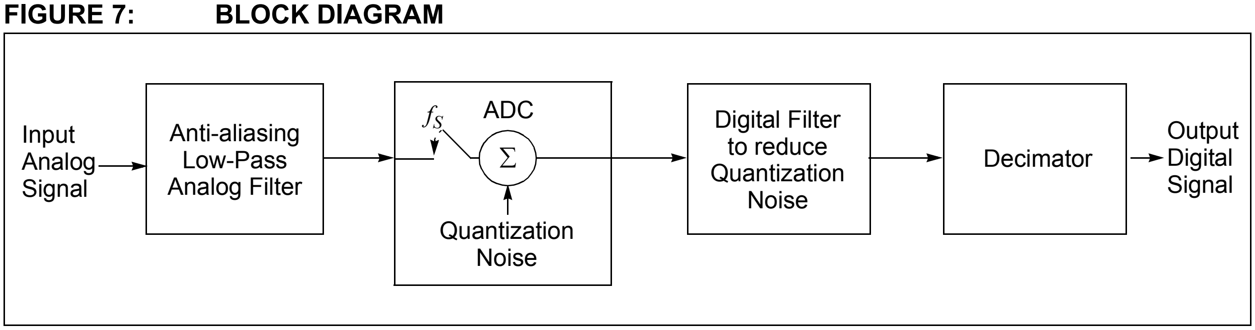
A low-pass FIR filter is used to filter the quantization noise from the analog-to-digital converted signal. The cut-off frequency of the FIR filter used is f_C. The order of the FIR filter can be set to O, $L = O + 1$ coefficients. The sampling frequency used can be set to $K \bullet f_N$, where $f_N = 2\,f_C$.

After filtering, the analog-to-digital converted signal is passed through a decimation stage to downgrade the rate, at which time the signal is sampled. The signal ultimately obtained has a higher SNR, which is close to the SNR of a *Q*-bit ADC although a *P*-bit ADC was employed for analog-to-digital conversion.

The block diagram of all the associated stages is shown in Figure 7.

Additional improvement in accuracy can be gained by adding an external dithering circuit before the ADC. Dithering is a technique used to minimize the ADC quantization noise by adding noise to the analog signal before passing it through the ADC. The periodicity of the quantization error in Figure 1 shows that it contains spectral harmonics, which yields the quantization noise highly correlated. Spectral harmonics make the filtering more difficult and results in residual components. Dithering makes the resulting quantization noise more random with reduced levels of undesirable spectral harmonics. The simple dithering circuit consists of a noise diode and an amplification stage.

FIGURE 7: BLOCK DIAGRAM



APPLICATION EXAMPLE

This section describes an example of a real-world application, upon which the techniques described in this application note can be used.

The application circuit consists of a sensor (force, pressure, humidity, etc.), a conditioning circuit and the dsPIC DSC, as shown in Figure 8.

The conditioning circuit used is a three op amp instrumentation amplifier as shown in Figure 9. Using a conditioning circuit, the two low-voltage signals from the differential output of the sensor are subtracted to produce a single-ended output signal. The result of this subtraction is amplified using a certain amount of gain so that it matches the input range of the ADC. The associated equations are included in Figure 9.

The implementation of the subtraction and gain functions are done so that the sensor signal is not contaminated with additional errors and matches the voltage range of the ADC. The amplified signal is fed to the ADC pin of the dsPIC DSC. As previously discussed, the dsPIC DSC does the oversampling, filtering and decimation to achieve accuracy improvement.

In this application example, an FSG15N1A differential output force sensor with a specific response time (i.e., the time required for the force sensor output to rise from 10% to 90% of the final value when subjected to change in force) is used.

The anti-aliasing filters associated with the decimation stage and the conditioning circuit (if any) are designed to filter the force sensor signal, which is sampled at a sampling frequency that is same as the response frequency = (1/response time). For example, if the response time is 1 ms, the sampling frequency must be at least 1 kHz. The cut-off frequency for the FIR anti-aliasing filter can be chosen to be slightly less than 500 Hz, assuming that the force sensor reading is recorded at a sampling frequency of 1 kHz.

The ADC is oversampled by a sampling factor, $K = 256$, to achieve the SNR rating of a 16-bit ADC from the 12-bit ADC signal. The ADC is oversampled using the sampling frequency of $f_{OS} = 256 \cdot f_N = 256$ kHz. An improvement of ~24 dB is expected using this technique.

FIGURE 8: BLOCK DIAGRAM WITH dsPIC® DIGITAL SIGNAL CONTROLLER

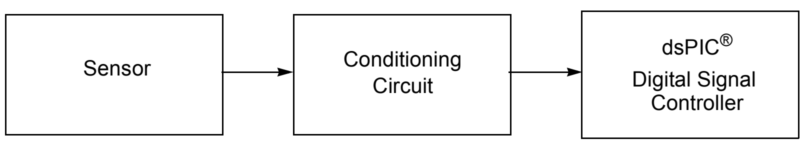
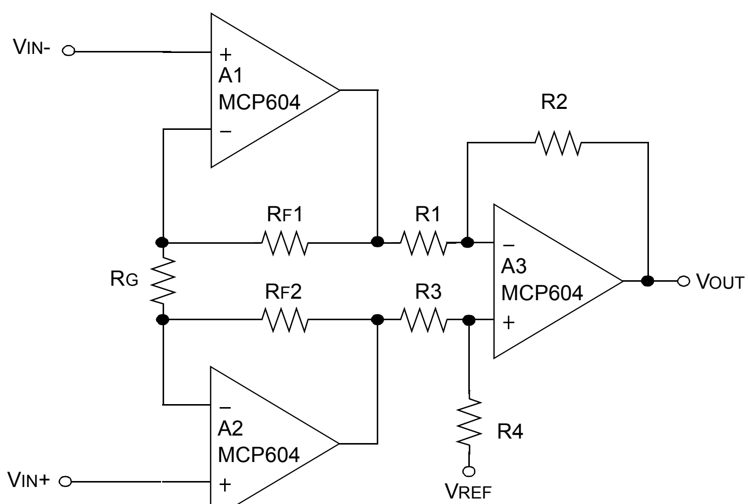


FIGURE 9: CONDITIONING CIRCUIT: THREE OP AMP INSTRUMENTATION AMPLIFIER



where: $R_{F1} = R_{F2}$ and $R_1 = R_2 = R_3 = R_4$

$$V_{OUT} = \left(1 + \frac{2R_F}{R_G}\right)(V_{IN+} - V_{IN-}) + V_{REF}$$

CONCLUSION

The accuracy of a low-resolution ADC can be improved by oversampling the input signal using the ADC and subjecting it to low-pass filtering, using a FIR filter to filter out the quantization noise, and then decimating it.

A dsPIC DSC device is ideal for this purpose, due to its DSC architecture, which enables DSP capability.

In our experiments, an average improvement of ~15 dB was seen when the input signal was oversampled by a factor of 256 using a 12-bit ADC and filtered using a regular FIR filter. This is an increase of 2.2 in effective number of bits (ENOB). A filter with tighter frequency cut-off will be able to provide the full 4-ENOB improvements with the 12-bit ADC.

REFERENCES

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Bonnie Baker - Application note, AN695 "*Interfacing Pressure Sensors to Microchip's Analog Peripherals*", Microchip Technology Inc., 2000.

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