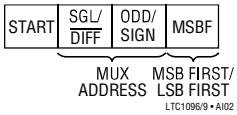
APPLICATION INFORMATION

Input Data Word

The LTC1286 requires no D_{IN} word. It is permanently configured to have a single differential input. The conversion result appears on the D_{OUT} line. The data format is MSB first followed by the LSB sequence. This provides easy interface to MSB or LSB first serial ports. For MSB first data the $\overline{CS}$ signal can be taken high after B0 (see Figure 1). The LTC1298 clocks data into the D_{IN} input on the rising edge of the clock. The input data words are defined as follows:



Start Bit

The first "logical one" clocked into the D_{IN} input after $\overline{CS}$ goes low is the start bit. The start bit initiates the data transfer. The LTC1298 will ignore all leading zeros which precede this logical one. After the start bit is received, the remaining bits of the input word will be clocked in. Further inputs on the D_{IN} pin are then ignored until the next $\overline{CS}$ cycle.

Multiplexer (MUX) Address

The bits of the input word following the START bit assign the MUX configuration for the requested conversion. For a given channel selection, the converter will measure the voltage between the two channels indicated by the + and – signs in the selected row of the following tables. In single-ended mode, all input channels are measured with respect to GND.

LTC1298 Channel Selection

	MUX ADDRESS		CHANNEL #		
	SGL/$\overline{DIFF}$	ODD/SIGN	0	1	GND
SINGLE-ENDED MUX MODE	1	0	+		–
	1	1		+	–
DIFFERENTIAL MUX MODE	0	0	+	–	
	0	1	–	+	

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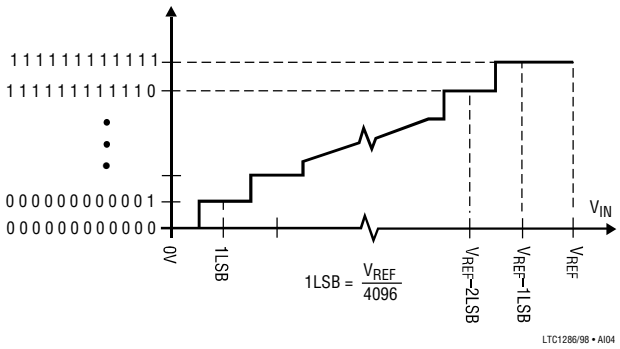
MSB First/LSB First (MSBF)

The output data of the LTC1298 is programmed for MSB first or LSB first sequence using the MSBF bit. When the MSBF bit is a logical one, data will appear on the D_{OUT} line in MSB first format. Logical zeros will be filled in indefinitely following the last data bit. When the MSBF bit is a logical zero, LSB first data will follow the normal MSB first data on the D_{OUT} line. (see Operating Sequence)

Transfer Curve

The LTC1286/LTC1298 are permanently configured for unipolar only. The input span and code assignment for this conversion type are shown in the following figures.

Transfer Curve



Output Code

OUTPUT CODE	INPUT VOLTAGE	INPUT VOLTAGE (V_{REF} = 5.000V)
111111111111111	V_{REF} – 1LSB	4.99878V
111111111111110	V_{REF} – 2LSB	4.99756V
•	•	•
•	•	•
•	•	•
000000000000001	1LSB	0.00122V
000000000000000	0V	0V

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Operation with D_{IN} and D_{OUT} Tied Together

The LTC1298 can be operated with D_{IN} and D_{OUT} tied together. This eliminates one of the lines required to communicate to the microprocessor (MPU). Data is transmitted in both directions on a single wire. The processor pin connected to this data line should be configurable as either an input or an output. The LTC1298 will take control of the data line and drive it low on the 4th falling CLK edge after the start bit is received (see Figure 3). Therefore the processor port line must be switched to an input before this happens to avoid a conflict.

In the Typical Applications section, there is an example of interfacing the LTC1298 with D_{IN} and D_{OUT} tied together to the Intel 8051 MPU.

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