PIC18F97J60 FAMILY

64/80/100-Pin High-Performance, 1-Mbit Flash Microcontrollers with Ethernet

Ethernet Features:

- IEEE 802.3 compatible Ethernet Controller
- Integrated MAC and 10Base-T PHY
- 8-Kbyte Transmit/Receive Packet Dual Port Buffer SRAM
- Receiver and Collision Squelch Circuit
- Supports one 10Base-T Port with Automatic Polarity Detection and Correction
- Programmable Automatic Retransmit on Collision
- Programmable Padding and CRC Generation
- Programmable Automatic Rejection of Erroneous Packets
- Activity Outputs for 2 LED Indicators
- Buffer:
  - Configurable transmit/receive buffer size
  - Hardware-managed circular receive FIFO
  - Byte-wide random and sequential access
  - Internal DMA for fast memory copying
  - Hardware-assisted IP checksum calculation
- MAC:
  - Support for Unicast, Multicast and Broadcast packets
  - Programmable pattern matching of up to 64 bytes within packet at user-defined offset
  - Programmable wake-up on multiple packet formats
  - Loopback mode
- PHY:
  - Wave shaping output filter
  - Loopback mode

Flexible Oscillator Structure:

- Selectable system clock derived from single 25 MHz external source:
  - 10 clock speeds from 2.78 to 41.67 MHz
- Internal 31 kHz oscillator
- Secondary oscillator using Timer1 @ 32 kHz
- Fail-Safe Clock Monitor:
  - Allows for safe shutdown if oscillator stops
- Two-Speed Oscillator Start-up

External Memory Bus (100-pin devices only):

- Address capability of up to 2 Mbytes
- 8-bit or 16-bit interface
- 12-bit, 16-bit and 20-bit Addressing modes

Peripheral Highlights:

- High current sink/source 25 mA/25 mA
- Five Timer modules (Timer0 to Timer4)
- Four external interrupt pins
- Two Capture/Compare/PWM (CCP) modules
- Three Enhanced Capture/Compare/PWM (ECCP) modules:
  - One, two or four PWM outputs
  - Selectable polarity
  - Programmable dead time
  - Auto-Shutdown and Auto-Restart
- Up to two Master Synchronous Serial Port (MSSP) modules supporting SPI™ (all 4 modes) and I^2C™ Master and Slave modes
- Two Enhanced USART modules:
  - Supports RS-485, RS-232 and LIN 1.2
  - Auto-Wake-up on Start bit
  - Auto-Baud Detect
- 10-bit, up to 16-channel Analog-to-Digital Converter module (A/D):
  - Auto-acquisition capability
  - Conversion available during Sleep
- Dual analog comparators with input multiplexing
- Parallel Slave Port (PSP) module (100-pin devices only)

Special Microcontroller Features:

- 5.5V Tolerant Inputs (digital-only pins)
- Low-power, high-speed CMOS Flash technology:
  - Self-reprogrammable under software control
- C compiler optimized architecture for re-entrant code
- Power Management Features:
  - Run: CPU on, peripheral on
  - Idle: CPU off, peripherals on
  - Sleep: CPU off, peripherals off
- Priority levels for interrupts
- 8 x 8 Single-Cycle Hardware Multiplier
- Extended Watchdog Timer (WDT):
  - Programmable period from 4 ms to 131s
- Single-Supply 3.3V In-Circuit Serial Programming™ (ICSP™) via two pins
- In-Circuit Debug (ICD) with 3 breakpoints via two pins
- Operating voltage range of 2.0V to 3.6V (3.14V to 3.45V using Ethernet module)
- On-chip 2.5V regulator

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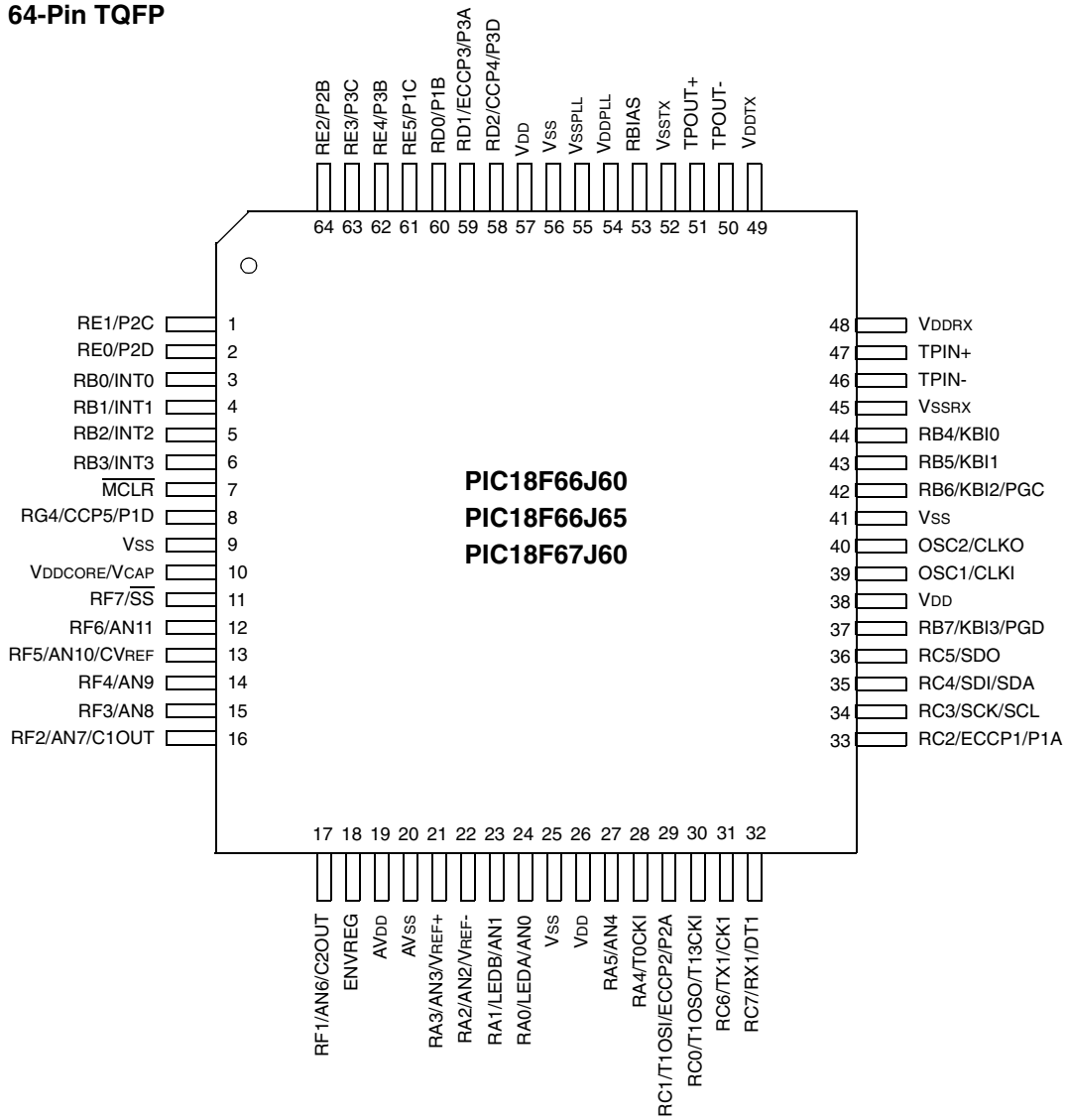
Device	Flash Program Memory (bytes)	SRAM Data Memory (bytes)	Ethernet TX/RX Buffer (bytes)	I/O	10-bit A/D (ch)	CCP/ ECCP	MSSP		EUSART	Comparators	Timers 8/16 bit	PSP	External Memory Bus
								SPI™	Master I^2C™					
PIC18F66J60	64 K	3808	8192	39	11	2/3	1	Y	Y	1	2	2/3	N	N
PIC18F66J65	96 K	3808	8192	39	11	2/3	1	Y	Y	1	2	2/3	N	N
PIC18F67J60	128 K	3808	8192	39	11	2/3	1	Y	Y	1	2	2/3	N	N
PIC18F86J60	64 K	3808	8192	55	15	2/3	1	Y	Y	2	2	2/3	N	N
PIC18F86J65	96 K	3808	8192	55	15	2/3	1	Y	Y	2	2	2/3	N	N
PIC18F87J60	128 K	3808	8192	55	15	2/3	1	Y	Y	2	2	2/3	N	N
PIC18F96J60	64 K	3808	8192	70	16	2/3	2	Y	Y	2	2	2/3	Y	Y
PIC18F96J65	96 K	3808	8192	70	16	2/3	2	Y	Y	2	2	2/3	Y	Y
PIC18F97J60	128 K	3808	8192	70	16	2/3	2	Y	Y	2	2	2/3	Y	Y

Pin Diagrams

64-Pin TQFP



Pinouts are preliminary and subject to change.

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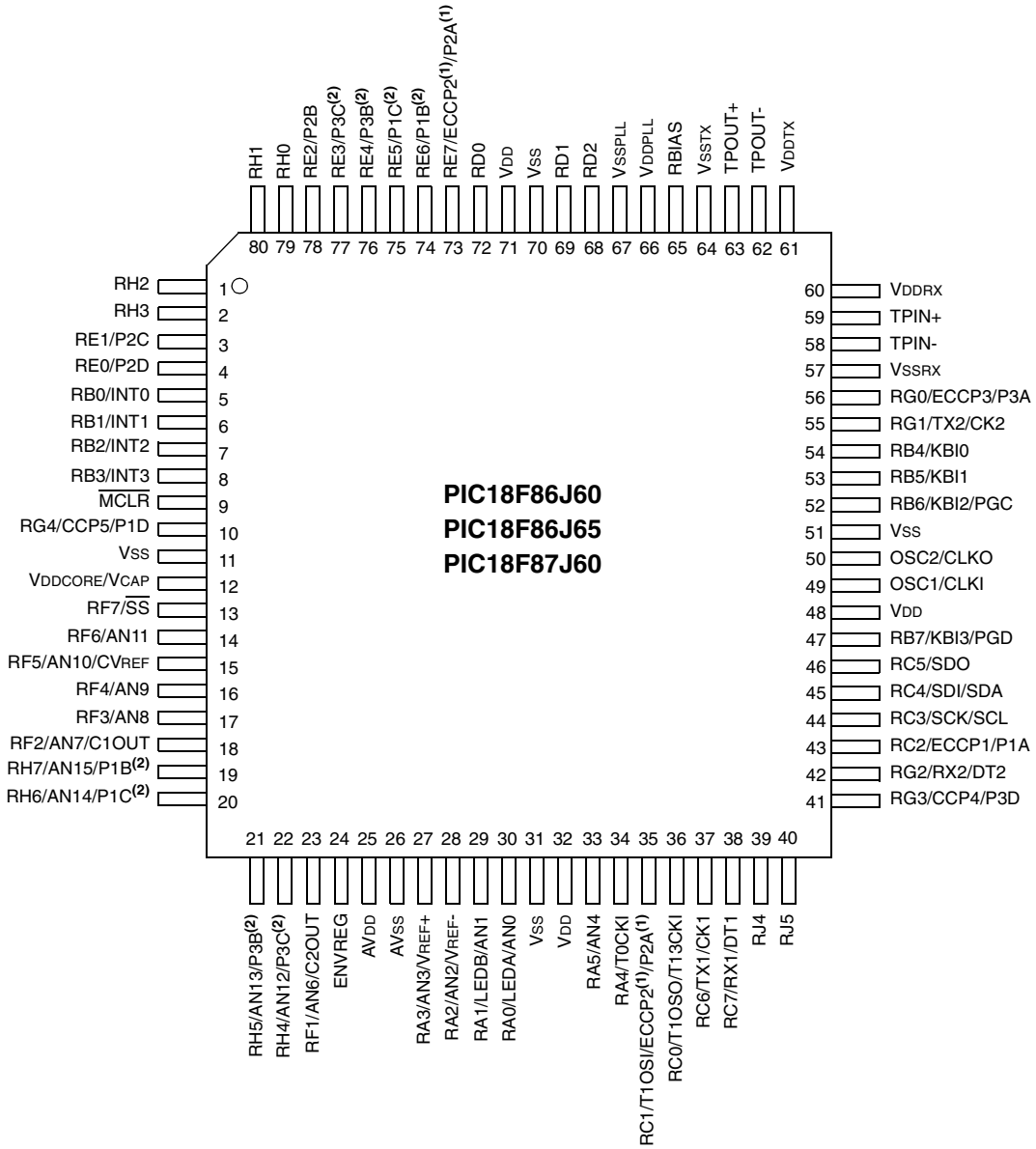
Pin Diagrams (Cont'd.)

80-Pin TQFP

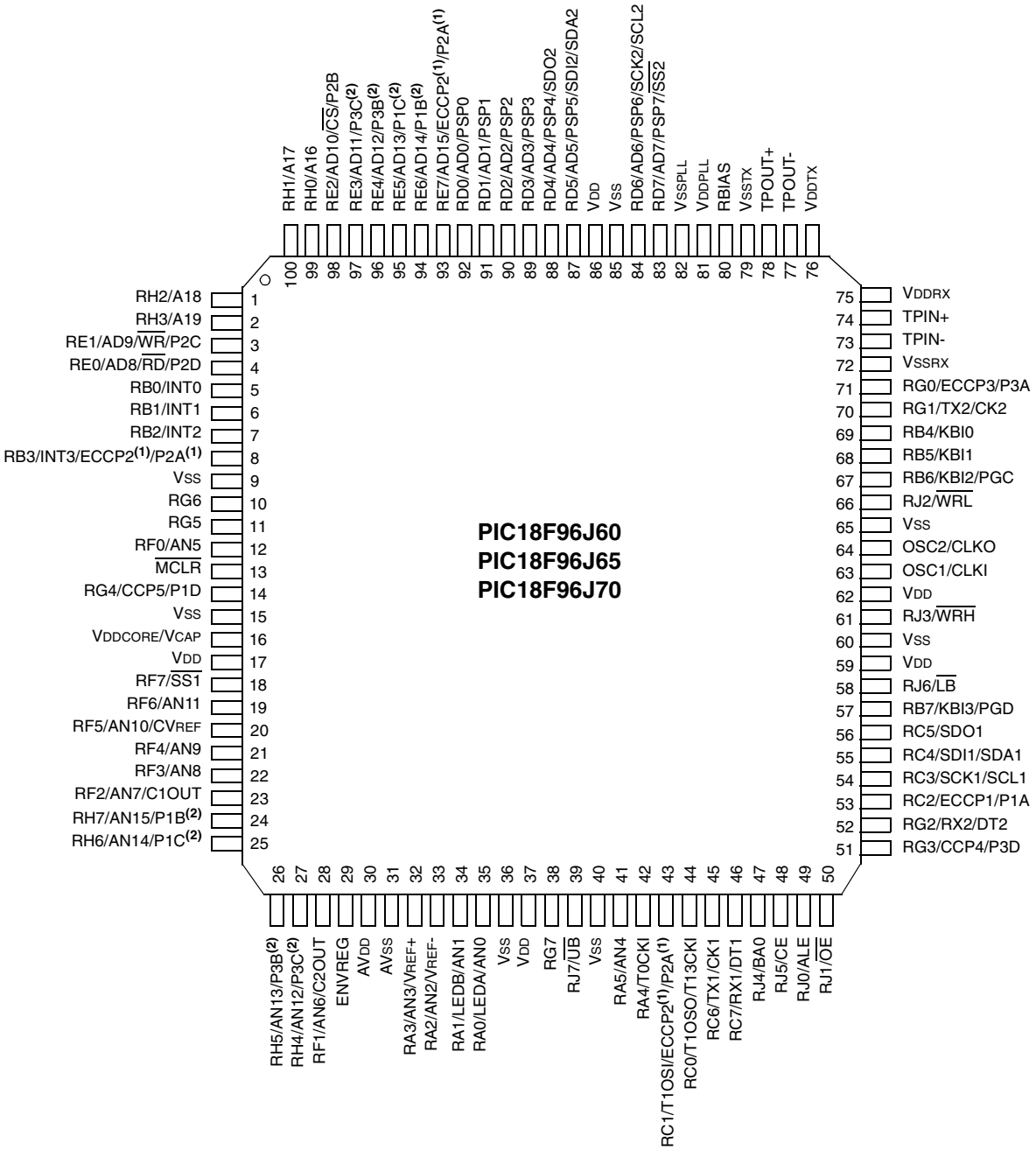


Pinouts are preliminary and subject to change.

Note 1: The ECCP2/P2A pin placement depends on the CCP2MX configuration bit settings.
2: P1B, P1C, P3B and P3C pin placement depends on the ECCPMX configuration bit setting.

Pin Diagrams (Cont'd.)

100-Pin TQFP



Pinouts are preliminary and subject to change.

Note 1: The ECCP2/P2A pin placement depends on the CCP2MX configuration bit and Processor mode settings.
2: P1B, P1C, P3B and P3C pin placement depends on the ECCPMX configuration bit setting.

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