SUNLIKE DISPLAY Model No :SG12864H

GENERAL SPECIFICATION

ITEM	DESCRIPTION				
Product No	SG12864HSLB-HB				
LCD Type	■ STN Gray Positive	☐ STN Yellow Green Positive	☐ STN Blue Negative		
	☐ FSTN Negative White & Black	☐ FSTN Positive Black & White			
Rear Polarizer	☐ Reflective	■ Transflective	☐ Transmissive		
Backlight Type	☐ NO B/L	■ LED	☐ CCFL	☐ EL	
Backlight Color	■ Yellow Green	☐ Green	☐ Amber	☐ White	☐ Blue Green
View Direction	■ 6 O'clock	☐ 12 O'clock			
Temperature Range	☐ Normal	■ Wide			
Frame	■ Black	☐ Silver			

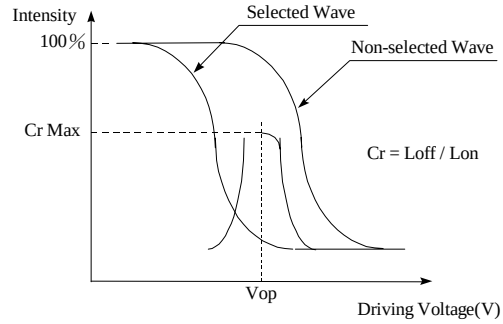
TO BE VERY CAREFUL !

The LCD driver ICs are made by CMOS process, which are very easy to be damaged by static charge, make sure the user is grounded when handling the LCM.

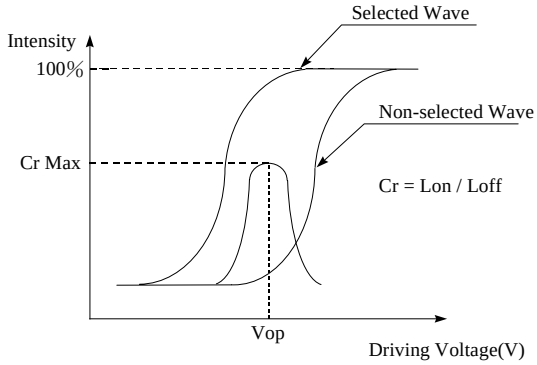
INTERFACE PIN ASSIGNMENT

PIN NO.	PIN OUT	LEVEL	FUNCTION DESCRIPTION
1	V_{DD}	5V	Power Supply Voltage
2	V_{SS}	0V	Power Supply Ground
3	V_O	---	Contrast Adjustment Voltage
4	DB0	H/L	Data Bit 0
5	DB1	H/L	Data Bit 1
6	DB2	H/L	Data Bit 2
7	DB3	H/L	Data Bit 3
8	DB4	H/L	Data Bit 4
9	DB5	H/L	Data Bit 5
10	DB6	H/L	Data Bit 6
11	DB7	H/L	Data Bit 7
12	CS1	H	Chip Select Signal For IC1
13	CS2	H	Chip Select Signal For IC2
14	/RES	L	Reset Signal
15	R/W	H/L	H : Read / L : Write
16	D/I	H/L	H : Data , L : Instruction Code
17	E	H→L	Enable Signal
18	Vout	---	Power Supply Voltage for LCD
19	A	4.2V	LED Power (＋)
20	K	0V	LED Power (－)

[Note 7] Definition of Operation Voltage (Vop)

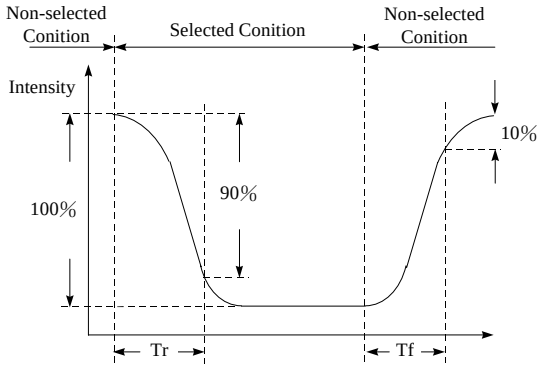


[positive type]

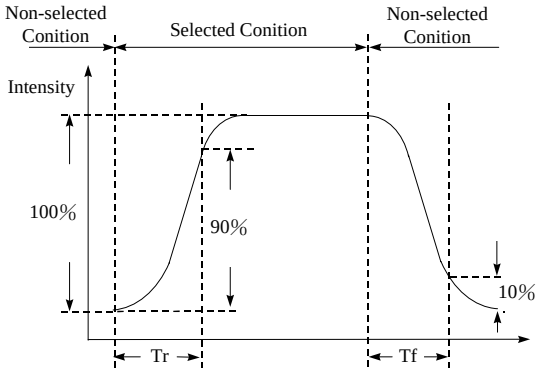


[Negative type]

[Note 8] Definition of Response Time (Tr, Tf)



[positive type]



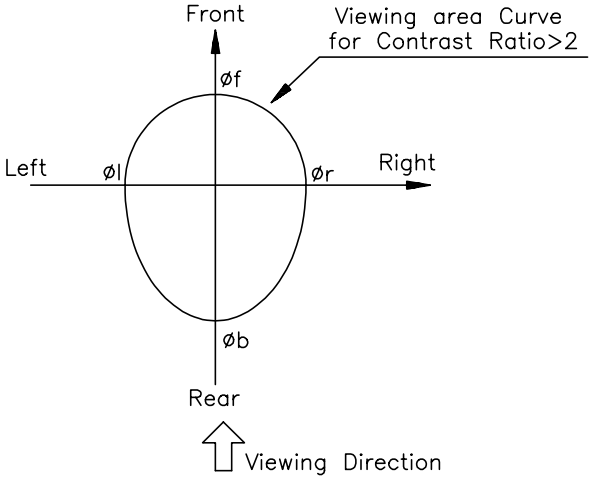
[Negative type]

Conditions:

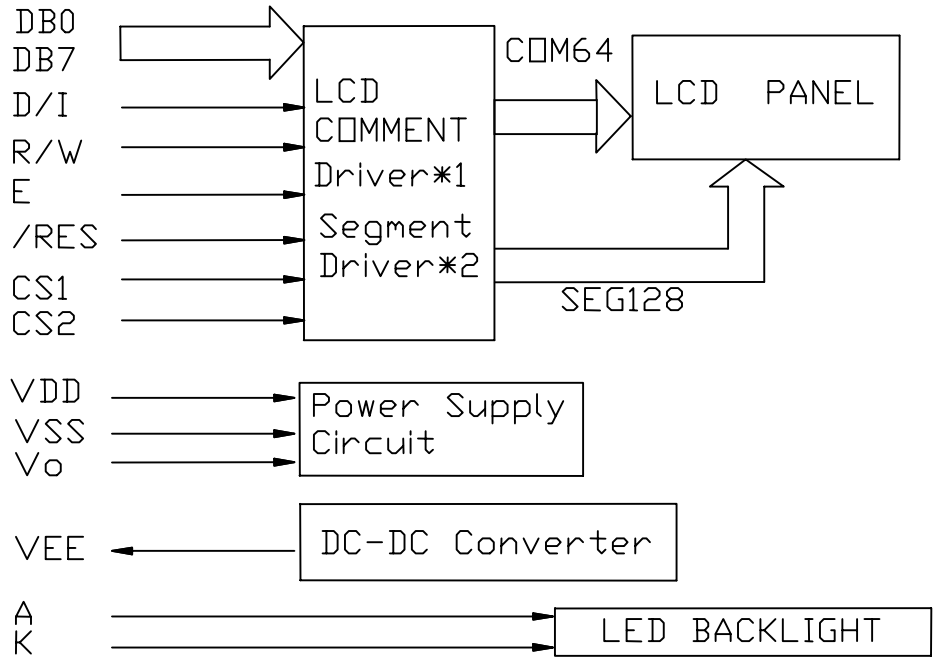
Operating Voltage : Vop **Viewing Angle(θ , φ): 0° , 0°**

Frame Frequency : 64 Hz **Driving Wave form : 1/N duty, 1/a bias**

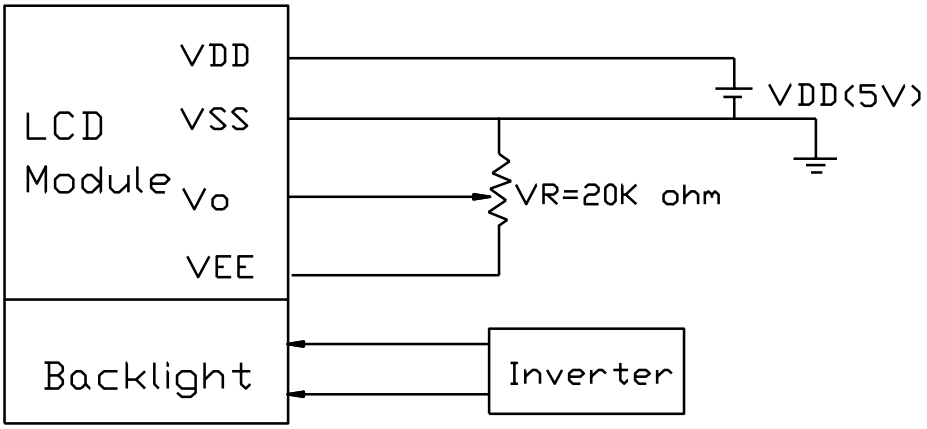
[Note 9] Definition of Viewing Direction



BLOCK DIAGRAM



POWER SUPPLY



INSTRUCTION CODE

NO	Instruction	Code										Function
		D/I	R/W	D7	D6	D5	D4	D3	D2	D1	D0	
1	Display ON / OFF	0	0	0	0	1	1	1	1	1	1/0	Controls display 0N/0FF. RAM data and internal status are not affected. 1: NO , 0: OFF
2	Display Start Line	0	0	1	1	Display start line (0-63)						Specifies the RAM line displayed at the top of the screen.
3	Page Address Set	0	0	1	0	1	1	1	Page (0-7)			Sets the page (X address) of RAM at the page (X address) register.
4	Set Address	0	0	0	1	Column Address (0-63)						Sets the Column (Y address) in the Column (Y address) counter.
5	Status Read	0	1	BUSY	0	ON/OFF	RESET	0	0	0	0	Reads the status. RESET 1: Reset 0: Normal ON/OFF 1: Display OFF 0: Display ON BUSY 1: Internal operation 0: Ready
6	Write Display Data	1	0	Write DATA								Write data DB0 to DB7 on the data bus into display RAM.
7	Read Display Data	1	1	Read DATA								Reads data DB0 to DB7 from the display RAM to the data bus.

* Initialization at power-on is performed not by the reset Instruction but by a reset signal applied to the RES pin.

Initialization

(a) Display off .

(b) Display start line register : First line .

(c) Static drive off .

(d) Column address counter : Address 0 .

(e) Page address register : Page 0 .

(f) Select duty : 1/64 duty

(1) Display On / Off

This command turns the display on and off no relation with the data in the display data RAM internal conditions.

Code

D/I	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	0	1	1	1	1	1	D

D 1: Display ON
0 : Display OFF

(2) Display Start Line

This instruction set the line address as shown Fig 1. The selected line the display data RAM correspond to the COM0 which display at the top of LCD panel . The display area is set automatically from the selected line to the line which increased the number of duty ratio . Therefore , the smooth scroll for vertical direction by changing the start line address one by one or page switching are available by this instruction .

Code

D/I	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	1	A5	A4	A3	A2	A1	A0

A5	A4	A3	A2	A1	A0	Line Address
0	0	0	0	0	0	0
					1	1
				1		2
1	1	1	1	1	0	3E
1	1	1	1	1	1	3F

(3) Page Address Set

When MPU access the Display Data RAM , the page address corresponded to the row address must be selected . The access in the Display Data RAM is available by setting the page and column address . (Refer the Fig . 1) The display is no change when the page address is changed .

Code

D/I	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	1	0	1	1	1	A2	A1	A0

A2	A1	A0	Page
0	0	0	0
0	0	1	1
1	1	0	6
1	1	1	7

(4) Column Address Set

This instruction set the column address in the display Data RAM . (see Fig . 1)

When the MPU access the Display Data RAM continuously , the column address increase "1" automatically , therefore , the MPU can access the data only without address setting . The increment of the column address is stopped by the address of 50H automatically , but the page address is no change even if the column address increase to 50H and stop .

Code

D/I	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	0	0	A6	A5	A4	A3	A2	A1	A0

A6	A5	A4	A3	A2	A1	A0	Column Address
0	0	0	0	0	0	0	0
						1	1
					1		2
1	1	1	1	1	1	0	3E
1	1	1	1	1	1	1	3F

(5) Status Read

This instruction read out internal status.

Code

D/I	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
0	1	Busy	0	on/off	Reset	0	0	0	0

Busy : Busy =1 : indicate the operating or the Reser cycle . The instruction can be input after the Busy status change to "0" .

On/Off : Indicate the whole display On/Off status .

0 : Whole display "On"

1 : Whole display "Off"

(Note) The data "0=On" and "1=Off" of Display On/Off status read out is inverted with the Display On/Off instruction data of "1=On" and "0=Off" .

Reset : Indicate the initialization period by /RST signal or reset instruction .

0 : ----

1 : Initialization period .

(6) Write Display Data

This instruction writes the 8-bits data on the data bus into the Display Data RAM . The column (segment) address increase "1" automatically when writing , therfore , the MPU can write the 8-bit data into Display Data RAM without address setting .

Code

D/I	R/W	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	0	Write Data							

(7) Read Display Data

This instruction read out the 8-bits data from Display Data RAM which addressed by the column and page address . in case of the Read Modify Write Mode is off , the column address increase "1" automatically after each read out , therefore , the MPU can read out 8-bit data from the Display Data RAM continuously without address setting . One time dummy read be required after column address set as explain in (4-3) .

Code

D/I	WR	DB7	DB6	DB5	DB4	DB3	DB2	DB1	DB0
1	1	Read Data							

Display Data Ram Addressing

Page Addrees cs1,cs2	Data	Display Pattern	Line Address
B8	D0	■ ■	C0
	D1	■ ■	C1
	D2	■ ■ ■	C2
	D3	■ ■ ■ 0 Page	C3
	D4	■ ■ ■	C4
	D5	■ ■	C5
	D6	■ ■	C6
	D7		C7
B9	D0		C8
	D1		C9
	D2		CA
	D3	1 Page	CB
	D4		CC
	D5		CD
	D6		CE
	D7		CF
BA	D0		D0
	D1	2 Page	D1
	D2		D2
	D3		D3
	D4		D4
	D5		D5
BE	D6	6 Page	F6
	D7		F7
BF	D0		F8
	D1		F9
	D2		FA
	D3	7 Page	FB
	D4		FC
	D5		FD
	D6		FE
	D7		FF
Column address		40 41 42 43 44 45 46 ... 7E 7F	
Segment Term		1 2 3 4 5 6 7 ... 63 64	

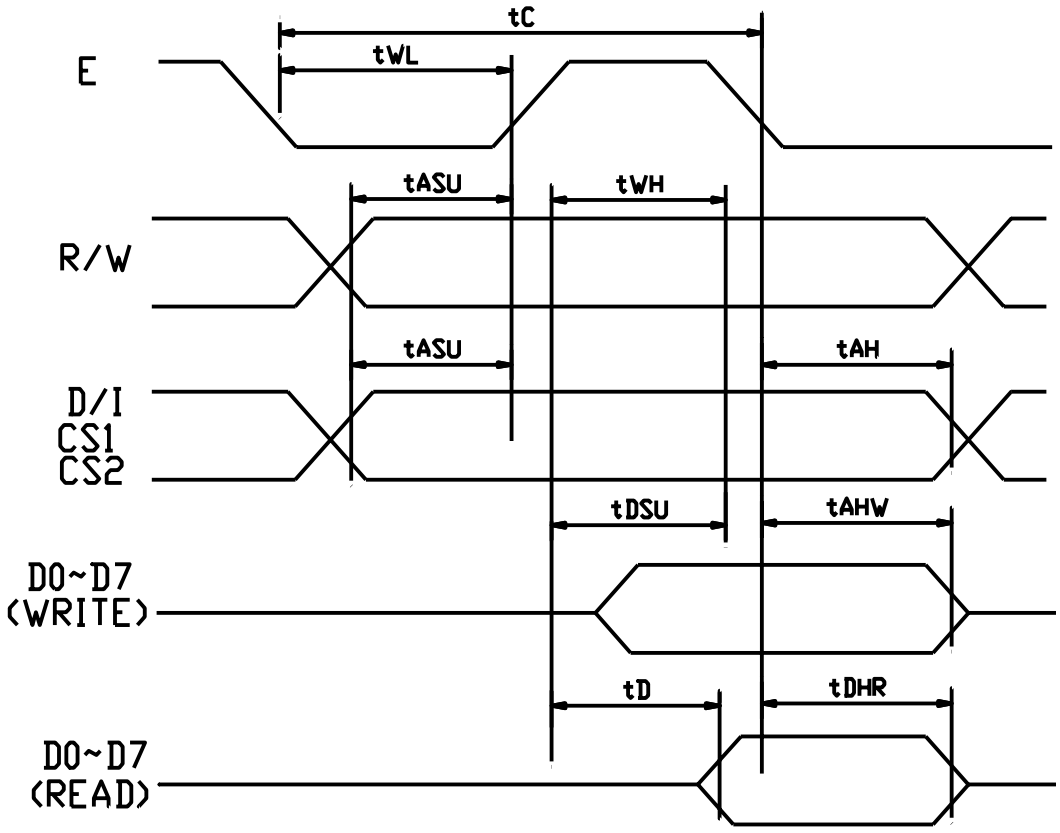
Fig.1Correspondence with display data RAM and address (For example the display start line is 10^{th} and 1/64 duty)

BUS TIMING CHARACTERISTICS

1. Read/Write operation seguence (68 type MPU)

(V_{DD}=5.0V±10%,V_{SS}=0V,Ta=-20~+75℃)

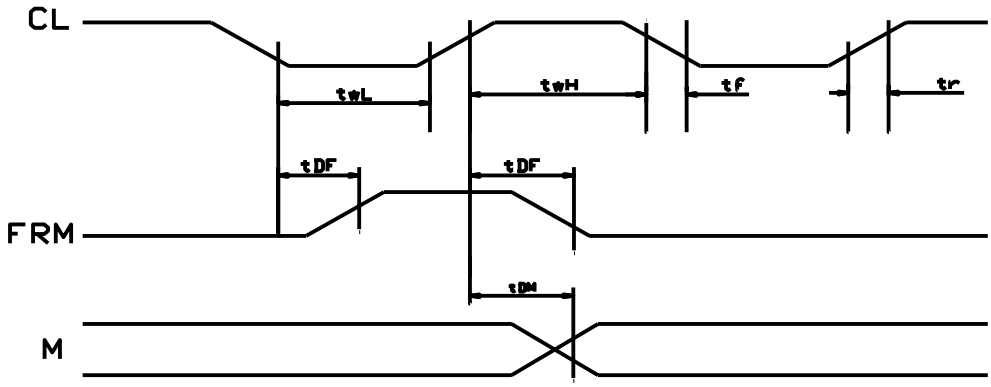
Parameter			Symbol	min	max	Condition	Unit
Address set up time		D/I,R/W Terminals	t_{ASU}	140	----	----	ns
Address hold time			t_{AH}	10	----		
System cycle time			t_C	1000	----		
Enable Pulse write	Low	E Terminal	t_{WL}	450	----		
	High		t_{WH}	450	----		
Data set up time		D0~D7 Terminals	t_{DSU}	200	----		
Data hold time			t_{DHW}	10	----		
Access time			t_D	----	320		
Output disable time			t_{DHR}	20	----		



2.Display control timing characteristics (68 type MPU)

(VDD=5.0V±10%,VSS=0V,Ta=-20~+75℃)

Parameter	Symbol	min	typ	max	Condition	Unit
"L" level pulse write	t_{WL}	35				us
"H" level pulse write	t_{WH}	35				
Ruse time	t_r		30	150		ns
Fall time	t_f		30	150		
FRM delay time	t_{DF}	-2.0		2.0		us
M delay time	t_{DM}	-2.0		2.0		



OPERATING PRINCIPLES & METHODS

1.Output register

Output register stores the data temporarily from display data RAM when CS1,CS2 is in active mode and R/W and D/I=H, stored data in display data RAM is latched in output register. When CS1,CS2 is in active mode and R/W=H,D/I=L, status data (busy check) can read out.

To read the contents of display data RAM, twice access of read instruction is needed. In first access, data in display data RAM is latched into output register. In second access, MPU can read data which is latched. That is, to read the data in display data RAM, it needs dummy read. But status read is not needed dummy read.

D/I	R/W	FUNCTION
L	L	Instruction
	H	Status read (busy check)
H	L	Data write (from input register to display data RAM)
	H	Data read (from display data RAM to output register)

2.Reset

Reset can be initialized system by setting RES terminal at low level when turning power on. receiving instruction from MPU. When RES become low, following procedure is occured.

1.Display OFF

2.Display start line register become set by 0.

While RES is low, any instruction except status read can be accepted. Reset status appers at DB4. After DB4 is low, any instruction can be accepted.

The conditions of power supply at initial power up are shown in table 1.

Table 1. Power Supply Initial Conditions

Item	Symbol	Min	Typ	Max	Unit
Reset Time	t_{RS}	1.0	--	--	us
Rise Time	t_R	--	--	200	ns